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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/051,062	01/22/2002	Masao Ohwada	NEG-241US	1809

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EXAMINER	
BADERMAN, SCOTT T	

ART UNIT	PAPER NUMBER
2113	

DATE MAILED: 09/28/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/051,062	OHWADA, MASAO	
	Examiner	Art Unit	
	Scott T Baderman	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 January 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4,7,10,13 and 14* is/are rejected.

7)☒ Claim(s) *2,3,5,6,8,9,11 and 12* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 January 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Allowable Subject Matter

1. Claims 2, 3, 5, 6, 8, 9, 11 and 12 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claim 1, 4, 7, 10, 13 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen (5,544,332) in view of Gibson (6,553,512).

As in claims 1 and 7, Chen discloses a system for enabling facilitated analysis of malfunction on a PCI bus (i.e. deadlock), arranged in a computer device in which a processor unit (interpreted as either one of the master, slave or arbiter) is connected over the PCI bus to a plural number of PCI devices (Figures 1-3, Abstract), said system comprising: said plural PCI devices (i.e., masters), each of which, when operating as a PCI master device, activates a corresponding master operating signal (Figures 1 and 2, Abstract, column 3: line 65 – column 4:

line 2); and a PCI bus monitor circuit (deadlock detection) for monitoring data transfers from masters, wherein said PCI bus monitor circuit detects a deadlock when plural PCI master devices respond for one PCI cycle (i.e., at the same time) (Figures 2 and 3, Abstract, column 3: line 57 – column 4: line 33). However, Chen does not specifically disclose monitoring target devices or sending an error report signal. Gibson discloses a system for handling errors that deadlock a CPU, wherein if the deadlock can not resolved without issuing a bus error, then a bus error is issued and the CPU attempts to restart (Abstract).

It would have been obvious to a person skilled in the art at the time the invention was made to include monitoring target devices into the system taught by Chen above. This would have been obvious because Chen clearly teaches that, like multiple masters, the system also includes multiple slave (target) devices (Figure 1). Being that Chen teaches that it is possible that more than one master device will attempt to access the bus at the same time (Abstract), it would have been suggested to a person skilled in the art that, due to multiple slaves present, they too could also access the bus at the same time, thereby causing similar deadlock situations.

It would have also been obvious to a person skilled in the art at the time the invention was made to send an error report signal in response to detecting the deadlock in the system taught by Chen above. This would have been obvious because Gibson specifically teaches that triggering a bus error in response to detecting a deadlock is a traditional method of resolving a deadlock (column 1: lines 34-40).

As in claim 13, Chen discloses wherein said processor unit includes a micro-processor, a host bridge and a memory and wherein said target operating signal is sent from said host bridge to said PCI bus monitor circuit (Figures 1 and 2, column 1: line 23 – column 2: line 2).

As in claims 4 and 10, Chen discloses a system for enabling facilitated analysis of malfunction on a PCI bus (i.e. deadlock), arranged in a computer device in which a processor unit is connected over the PCI bus to a plural number of PCI devices (Figures 1-3, Abstract), said system comprising: said plural PCI devices (i.e., masters), each of which, when operating as a PCI master device, activates a corresponding master operating signal (Figures 1 and 2, Abstract, column 3: line 65 – column 4: line 2); and a PCI bus monitor circuit (deadlock detection) for monitoring data transfers from masters, wherein said PCI bus monitor circuit detects a deadlock when plural PCI master devices respond for one PCI cycle (i.e., at the same time) (Figures 2 and 3, Abstract, column 3: line 57 – column 4: line 33). However, Chen does not specifically disclose monitoring target devices or a means for resetting the PCI bus. Gibson discloses a system for handling errors that deadlock a CPU, wherein if the deadlock can not resolved without issuing a bus error, then a bus error is issued and the CPU attempts to restart (Abstract).

It would have been obvious to a person skilled in the art at the time the invention was made to include monitoring target devices into the system taught by Chen above. This would have been obvious because Chen clearly teaches that, like multiple masters, the system also includes multiple slave (target) devices (Figure 1). Being that Chen teaches that it is possible that more than one master device will attempt to access the bus at the same time (Abstract), it would

have been suggested to a person skilled in the art that, due to multiple slaves present, they too could also access the bus at the same time, thereby causing similar deadlock situations.

It would have also been obvious to a person skilled in the art at the time the invention was made to send an error report signal and restart the bus in response to detecting the deadlock in the system taught by Chen above. This would have been obvious because Gibson specifically teaches that triggering a bus error and resetting the bus in response to detecting a deadlock is a traditional method of resolving a deadlock (column 1: lines 34-40).

As in claim 14, Chen discloses wherein said processor unit includes a micro-processor, a host bridge and a memory and wherein said target operating signal is sent from said host bridge to said PCI bus monitor circuit (Figures 1 and 2, column 1: line 23 – column 2: line 2).

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

See Form PTO-892.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Scott T Baderman whose telephone number is (703) 305-4644. The examiner can normally be reached on Monday-Friday, 6:45 AM-4:15 PM, first Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (703) 305-9713. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Scott T Baderman
Primary Examiner
Art Unit 2113

STB